PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 216952WO	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US02/38989	International filing date *(day/month/year)* 31 December 2002 (31.12.2002)	Priority date *(day/month/year)* 31 December 2001 (31.12.2001)
International Patent Classification (IPC) or national classification and IPC IPC(7): H01L 21/306; C23F 1/00; B05C 11/00; C23C 14/32 and US Cl.: 204/192.13, 298.03; 156/345.25, 345.36, 345.27, 345.28; 216/59, 60, 61; 427/8, 9, 19; 118/663, 664, 665		
Applicant TOKYO ELECTRON LIMITED		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of Ø sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand 14 April 2003 (14.04.2003)	Date of completion of this report 03 March 2004 (03.03.2004)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Rodney G. McDonald Telephone No. 571-272-1300

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/38[illegible]

I. Basis of the report

1. With regard to the **elements** of the international application:*

☒ the international application as originally filed.

☒ the description:
pages 1-23 as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

☒ the claims:
pages 24-26 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

☒ the drawings:
pages 1-22 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/389[redacted]

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims	5-9, 17, 18 and 20-22	YES
	Claims	1-4, 10-16 and 19	NO
Inventive Step (IS)	Claims	5	YES
	Claims	1-4 and 6-22	NO
Industrial Applicability (IA)	Claims	1-22	YES
	Claims	NONE	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

V. 2. Citations and Explanations:
Claims 1-4, 10-16 and 19 lack novelty under PCT Article 33(2) as being anticipated by Farber et al. (U.S. Pat. 6,232,134).

Farber et al. teach a method and apparatus for characterizing processing operations is presented. Following exposure of a wafer to plasma, the surface charge distribution pattern on the wafer is measured. The surface charge distribution pattern on the wafer is then compared with known surface charge distribution patterns to determine if the measured charge distribution pattern correlates to desirable patterns associated with successful performance of one or more processing steps. In some embodiments, the comparison of the measured charge distribution pattern can be used to detect specific problems in one or more processing steps such that corrective action can be taken in a timely manner. The comparison between the measured charge distribution pattern and known charge distribution patterns may be performed using image comparison or using quantitative comparisons based on charge levels measured within each pattern. (Abstract)

The dielectric layer may be formed through deposition or through a process where the dielectric is grown on the surface of the wafer. The dielectric is preferably a material that has favorable charge retention characteristics such that measurements of retained charge on the surface of the wafer can be performed at various times following processing steps without substantially affecting the measured results. One such material that has favorable charge retention characteristics is a thermal oxide that includes silicon such as thermally grown silicon dioxide, which is commonly used as a gate dielectric in semiconductor integrated circuits. Other example dielectric layers include semiconductive films, polymers, nitride layers such as silicon nitride layers, and photoresist layers. (Column 3 lines 20-34)

At step 104, the wafer is exposed to plasma or some other charge-comprising environment. Such exposure may be performed in a processing tool that supports both collection of charge data and etching operations. Exposure to plasma in semiconductor processing operations is typically associated with etching operations, cleaning operations, or deposition operations. Exposure of the wafer to plasma at step 104 results in surface charge being induced on the wafer. The characteristics of the various levels of charge distributed at various points on the surface of the wafer, may be influence by a number of variables. Such variables include variables associated with the processing step that requires exposure of the wafer to plasma. Such processing steps typically are performed within a plasma chamber, radio frequency (RF) power used to generate and sustain the plasma, and variables associated with gas flow into the plasma chamber, the type of gas used in the plasma chamber, pressurization of the plasma chamber, the wafer position with respect to other portions of the plasma chamber, and those variables associated with the electric fields that are generated for guiding the plasma within the plasma chamber may all have differing effects on the distribution of charge on the surface of the wafer. (Column 3 lines 35-47)

In addition to the variables associated with the exposure to plasma, variables associated with the composition of the wafer at the time of exposure to the plasma may also influence the charge distribution pattern across the surface of the wafer. Such wafer dependent parameters may include the various types of materials included at various points on the wafer, general wafer topography, and specific geometrical structures formed at differing points on the wafer surface. (Column 3 lines 58-65)

At step 106, the surface charge distribution pattern on the wafer is measured or scanned. This step of collecting plasma charge data from the surface of the wafer or substrate can be used to provide an indication as to the successful or unsuccessful

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(To be used when the space in any of the preceding boxes is not sufficient)

performance of various processing steps used to process the wafer. In one embodiment, the plasma charge data can be used to determine etching characteristics of a given process step, where the etching characteristics may correspond to one of the charge retention materials described above. In another embodiment, the plasma charge data may be used to determine deposition characteristics of a given process step. (Column 3 lines 66-68; Column 4 lines 1-10)

Charge measurement devices that are capable of measuring the surface charge distribution pattern on the wafer are currently known in the art, but as indicated earlier, are only known to be used for detecting charge aberrations that may result in damage to circuit components on the wafer. The plasma charge data that is measured at step 106 may include at least one discrete point of data measured from the surface of the substrate, and may further include a plurality of charge data points measured across the surface of the substrate to obtain the charge distribution pattern. (Column 4 lines 11-20)

At step 108 the surface charge distribution pattern measured at step 106 is compared with at least one known charge distribution pattern. Preferably, the known charge distribution pattern is stored in a computer readable medium. The reference charge data included in the reference charge distribution patterns may be charge data collected from one or more previous wafers processed using the method, or may be data collected from a single master reference substrate. The known charge distribution pattern may be associated with a desirable reference charge distribution pattern that, if a positive comparison is determined, indicates that the processing step(s) being monitored has been performed successfully. In other embodiments, charge distribution patterns compared at step 108 may include those associated with problem reference charge distribution patterns such that variations in the charge distribution pattern associated with specific errors or faults at various points in the processing process can be recognized. (Column 4 lines 21-38)

Step 108 may be performed as illustrated at step 112 by performing an image based pattern comparison (optical pattern recognition process) between the surface charge distribution pattern that has been measured and known surface charge distribution patterns. By generating images corresponding to various charge distribution patterns, the images can be visually compared manually or compared using an image processing circuit or similar device in order to determine if aberrations in the images or other unexpected variations have occurred. FIGS. 2-4 provide graphical representations of various surface charge distribution patterns that may be used to aid in understanding the image based comparison process. (Column 4 lines 39-51)

The comparison step performed at step 108 may be refined based on additional feedback received from processed charge monitor wafers. Thus, if repeated use of the method illustrated in FIG. 1 produces resulting wafers that included integrated circuits that provide additional detail as to the correlation of the measured charge distribution on the wafer to the production of functional integrated circuits, the comparison step performed at step 108 may be adapted. Such adaptation may improve the comparison step such that functional integrated circuits are more likely to be produced using the process step(s) monitored through the execution of the method of FIG. 1. Thus, the comparison may be adjusted in accordance with substrate integrated circuit yield data to adjust comparison rules in a manner that improves yield. (Column 6 lines 44-52)

Finally, at step 110 process parameters are evaluated based on the result of the comparison. This may include determining whether etching characteristics associated with the processing step being monitored are acceptable. Characterization of the etching characteristics may include determining a uniformity of an etch rate across the substrate, or determining the selectivity of the etch rate across the substrate. In some example applications, the etching characteristics may be used to determine if a profile of a via has been properly etched, if the topography of the surface of the substrate is acceptable, to calibrate an etch chamber to an acceptable initial condition, to determine microloading etch characteristics associated with etching a material on a substrate, and to correlate etching operations in two or more etching chambers such that the chambers process substrates with close consistency. (Column 6 lines 58-68; Column 7 lines 1-6)

If the comparison performed at step 108 indicates that the processing steps performed have been performed in an acceptable manner, the current configuration of the processing equipment may be maintained such that future wafers processed in a similar manner are likely to be processed in an acceptable manner. However, if the results of the comparison at step 108 indicate that deviations exists within the process parameters that are undesirable, processing steps or equipment may be modified or adjusted and additional evaluation performed prior to subsequent processing of production wafers. (Column 7 lines 7-17)

At step 506, the process step being performed is being characterized with regard to the process qualification wafer. Note that various techniques can be used to perform the characterization at step 506. Such techniques may include both manual and automated techniques. In the example where the process qualification wafer includes vias or similar structures, the characterization step performed at step 506 may include cutting the wafer into cross sectional portions such that manual or automated measurements can be taken to determine the process parameters corresponding to the processing step. Such processing steps may include monitoring different variables with respect to steps such as etching steps. Such variables corresponding to the etching steps may include etching rates, uniformity of etching across the wafer, selectivity of etch rate across the wafer, and an etch profile across the wafer. Selectivity of etching may include determining an etching rate with respect to one material that is being etched and comparing the rate of etching for that material with the rate of etching of additional materials. (Column 7 lines 57-68; Column 8 lines 1-9)

At step 508, the charge distribution pattern on the monitor wafer is measured. As described with respect to FIG. 1, the charge distribution pattern is preferably measured using a charge measurement instrument such as those currently known in the art. (Column 7 lines 57-68; Column 8 lines 1-9)

At step 510, the process characterization performed at step 506 is correlated with the measured charge distribution pattern obtained at step 508. Because the monitor wafer and the process qualification wafer are both exposed to the plasma under similar conditions in the same plasma environment, the characteristics resulting in the process qualification wafer as determined at step 506 can be correlated with the charge distribution pattern measured on the monitor wafer at step 508. As such, if a subsequent monitor

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wafer were exposed to the plasma in the same environment and produced a similar charge distribution pattern, a subsequently exposed process qualification wafer exposed to the plasma in the same environment should produce similar process parameter characterization data as that determined for the process qualification wafer characterized at step 506. (Column 8 lines 15-29)

In some instances, multiple process qualification wafers may have to be characterized in order to generate a sufficient data set to accurately correlate the process characterization with the different measured charge distribution patterns on different monitor wafers. Therefore, at step 512 it is determined whether or not sufficient correlation data has been obtained. If sufficient correlation data has not been obtained, the method returns at step 502 and the exposure, characterization, and charge distribution measurement steps are repeated iteratively until sufficient correlation data is determined to have been obtained at step 512. (Column 8 lines 30-41)

Once the reference charge distribution pattern(s) have been established at step 514, the method proceeds to step 520 where at least one wafer is manufactured using one or more of the reference charge distribution patterns established at step 514 to monitor process performance at one or more processing steps. Thus, at some subsequent point in time, a monitor wafer can be processed to determine if the processing operations are being performed within acceptable thresholds. Assuming that acceptable thresholds are achieved, a wafer that includes integrated circuits may be processed using the processing operations that have been judged acceptable. (Column 9 lines 11-22)

The memory 650 receives the current measured charged distribution pattern 650 for the wafer currently being monitored by the charge measurement instrument 610, and the processing module 622 performs a comparison between the current measured charge distribution pattern 650 and other charge distribution patterns stored within the memory 624. Based on the comparison performed, the processing module 622 determines a relationship between the current measured charge distribution pattern 650 and the reference patterns currently stored in the memory 624 to evaluate the processing operations performed on the wafer being monitored by the charge measurement instrument 610. Based on this comparison, the processor 620 generates an output 660. (Column 10 lines 21-34)

The output 660 may be an automated control signal that alters processing operations currently being performed, a signal to an operator in the semiconductor processing environment, or any other indication that could be used to facilitate proper processing of wafers. Generally, the output 660 should provide some type of signal that generates corrective measures for potentially problematic processing operations. Depending on the array of problem reference charge distribution patterns 640 stored within the memory 624, various levels of expected responses could be determined. (Column 10 lines 35-45)

A method for processing a substrate, the method comprising the steps of: collecting plasma charge data from a surface of the substrate; and using the plasma charge data to determine etching characteristics of a given process step. Wherein the plasma charge data is at least one discrete point of data measured from the surface of the substrate. Wherein the plasma charge data is a plurality of charge data points measured across the surface of the substrate to obtain a charge distribution pattern. Wherein the step of using comprises: comparing the plasma charge data to reference charge data stored in computer readable medium. Wherein the step of using comprises: comparing the plasma charge data to reference charge data stored in computer readable medium to determine whether the etching characteristics are acceptable. Wherein the etching characteristics include uniformity of an etch rate across the substrate. Wherein the etching characteristics include an etch rate across the substrate. Wherein the etching characteristics include a selectivity of the etch rate across the substrate. Wherein the comparing is performed by an optical pattern recognition process. (Column 11 lines 45-68; Column 12 lines 1-7)

The method of claim 5 wherein the step of comparing results in a comparison value, whereby if the comparison value is within at least one tolerance, the substrate is deemed to be acceptably processed, whereas if the comparison value is outside the at least one tolerance, the substrate is deemed to be unacceptably processed. (Column 12 lines 39-46)

Claims 1-4, 10-16 and 19 lack novelty under PCT Article 33(2) as being anticipated by Flamm et al. (U.S. Pat. 5,711,849).

Flamm et al. teach a method of designing a reactor 10. The present reactor design method includes steps of providing a first plasma etching apparatus 10 having a substrate 21 therein. The substrate includes a top surface and a film overlying the top surface, and the film having a top film surface. The present reactor design method also includes chemical etching the top film surface to define a profile 27 on the film, and defining etch rate data from the profile region. A step of extracting a reaction rate constant from the etch rate data, and a step of using the reaction rate constant in designing a second plasma etching apparatus is also included. (See Abstract)

A step of plasma etching the film is performed by step 101. The plasma etching step occurs at constant pressure and preferably constant plasma source characteristics. More preferably, the plasma etching step occurs isothermally at temperature T.sub.1, but can also be performed with changing temperatures where temperature and time histories can be monitored. Plasma etching of the film stops before the endpoint (or etch stop). Alternatively, plasma etching stops at a first sign of the endpoint (or etch stop). The plasma etching step preferably stops before etching into an etch stop layer underlying the film to define a "clean" etching profile. (Column 5 lines 16-26)

The substrate including etched film is removed from the chamber of the plasma etching apparatus. The etched film includes an etching profile (step 103) made by way of plasma etching (step 101). The etching profile converts into a relative etch rate, relative concentration ratio, a relative etch depth, and the like at selected spatial coordinates. The relative etch rate is defined as an etch rate at a selected spatial coordinate over an etch rate at the substrate edge. The relative concentration ratio is defined as a concentration of etchant species at a selected spatial coordinate over a concentration of etchant at the substrate edge. (Column 5 lines 27-37)

From the concentration and the surface reaction rate, the particular etching step can be improved by way of adjusting selected etching parameters. In an alternative specific embodiment, a method to "tune" a plasma source using a loading effect

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relationship (or equation) is illustrated by the simplified flow diagram 200 of FIG. 4. The method includes a step 201 of measuring an etch rate against an effective etchable area A.sub.w. The effective etchable area changes by varying the number m of wafers in the reactor, varying the size of the wafer, or the like. The effective area can be changed 209 by altering a gap between a wafer and its above surface 211, changing wafer quantity in the reactor 213, and varying substrate support member dimensions 215. The method preferably occurs at constant temperature and pressure. However, the effective etchable area may also be varied by way of changing a temperature and/or a pressure. The method calculated a uniformity value (step 217) from the measured values of etch rate vs. effective area in steps 211, 213 and 215. (Column 7 lines 23-41)

In step 207, the method changes plasma source parameters such as rf power, flow rate, and the like to select desired etching conditions. Once one of the aforementioned parameters is adjusted, the method returns to step 201 via branch 208. At step 201, an etch rate vs. effective etchable area is measured and the method continues through the steps until desired etching condition are achieved. Of course, other sequences of the aforementioned step for tuning the plasma source may also exist depending upon the particular application. (Column 8 lines 44-53)

FIG. 5 is a simplified flow diagram for a method of selecting a desired uniformity and desired etching parameters within selected ranges to provide a desired etch rate for a particular etching process. The etching parameters include process variables such as reactor dimensions, a pressure, a temperature, and the like for a particular substrate and reactants. Other etching parameters may also be used depending upon the particular application. (Column 8 lines 54-61)

Claims 1-4 and 6-22 lack an inventive step under PCT Article 33(3) as being obvious over Farber et al. (U.S. Pat. 6,232,134).

Farber is discussed above and all is as applies above. (See Farber discussed above)

The differences between Farber et al. and the present claims is that using multivariate analysis is not discussed, the parameter utilized is not discussed, is that the chamber being a photoresist coating chamber is not discussed, wherein the chamber being a dielectric coating chamber is not discussed, where the chamber is a lithography system is not discussed, where the chamber is a rapid thermal processing system is not discussed and where the chamber is a batch diffusion furnace is not discussed.

As to the multivariate analysis since Farber et al. suggest utilizing variables to control the process this would inherently "fit" a multivariate equation.

As to the chamber being a photoresist coating chamber, a dielectric coating chamber, a lithography system, a rapid thermal processing system and a batch diffusion furnace the process and apparatus is applicable to semiconductor manufacturing systems. (Column 1 lines 8-12) that includes etching cleaning, and deposition operations. (Column 3 lines 40-41)

The parameters utilized can include RF power, gas flow, etc. (Column 3 lines 47-57)

The motivation for utilizing multivariate equations, various chamber process configurations and parameters is that it allows for controlling the process to be within acceptable guidelines. (Column 2 lines 57-61)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Farber et al. by utilizing multivariate equations, various chamber process configurations and process parameter because it allows for controlling process to be within acceptable guidelines.

Claims 1-4 and 6-22 lack an inventive step under PCT Article 33(3) as being obvious over Flamm et al. (U.S. Pat. 5,711,849).

Flamm et al. is discussed above and all is as applied above. (See Flamm et al. discussed above)

The differences between Flamm et al. and the present claims is that using multivariate analysis is not discussed, the parameter utilized is not discussed, is that the chamber being a photoresist coating chamber is not discussed, wherein the chamber being a dielectric coating chamber is not discussed, where the chamber is a lithography system is not discussed, where the chamber is a rapid thermal processing system is not discussed and where the chamber is a batch diffusion furnace is not discussed.

As to the multivariate analysis since Farber et al. suggest utilizing variables to control the process this would inherently "fit" a multivariate equation.

As to the chamber being a photoresist coating chamber, a dielectric coating chamber, a lithography system, a rapid thermal processing system and a batch diffusion furnace the process and apparatus is applicable to semiconductor manufacturing systems. (Column 1 lines 1-16)

The parameters that can be utilized can include pressure, temperature, etc. (Column 8 lines 57-60)

The motivation for utilizing multivariate equations, various chamber process configurations and parameters is that it allows for design of reactors. (Column 1 lines 49-57)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Flamm et al. by utilizing multivariate equations, various chamber process configurations and parameters because it allows for designing of reactors.

Claim 5 meets the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach utilizing Fourier harmonics to achieve processing.

Claims 1-22 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made in industry for performing material processing.